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06ES32

Third Semester B.E. Degree Examination, June-July 2009
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least Two questions from each part.*
2. Make suitable assumptions if necessary.

PART - A

1 a. With respect to a semiconductor diode, explain the following:
i) Reverse Recovery time
ii) Diffusion capacitance. **(06 Marks)**

b. How does a clamping circuit differ from a clipping circuit? For the diode clipping circuit shown in Fig.1(b), draw the input and output waveforms for i) R = 100 Ω; ii) R = 1kΩ; iii) R = 10kΩ for $V_i = 20$ Sinwt and $V_R = 10V$. Assume Rf = 100Ω, Rr = ∞ and $V_\gamma = 0$. **(08 Marks)**

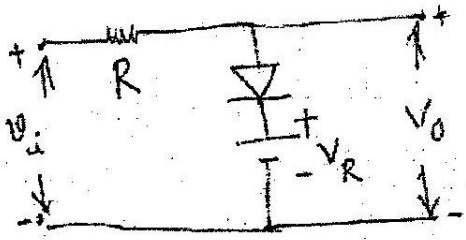

Fig.1(b).

c. Draw the circuit diagram of a full wave rectifier with capacitor filter. The circuit uses a capacitor of 1000 μF and provides a d.c. load current of 500 mA at 2% ripple. Assume f = 50Hz. Calculate i) D.C. output voltage; ii) Peak rectified voltage and % regulation. **(06 Marks)**

2 a. What is meant by transistor biasing? Compare different biasing methods used for transistor biasing with respect to stability. **(05 Marks)**

b. Find the operating point for the voltage divider bias circuit with β = 80 and $V_{BE} = 0.6V$. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25. Given V_{cc} = 15V, $R_1 = 100k\Omega$, $R_2 = 18k\Omega$, $R_c = 4.7k\Omega$, $R_E = 1k\Omega$. **(07 Marks)**

c. With the help of a neat circuit diagram, explain the use of transistor as an inverter. **(08 Marks)**

3 a. What are the advantages of using hybrid model to represent the transistor? Explain how h-parameters can be obtained from the static characteristics of the transistor. **(06 Marks)**

b. For the Emitter follower circuit, derive expressions for A_V, A_I, R_{in} and R_o of an emitter follower. **(08 Marks)**

c. Compare the characteristics of CE, CC, CB configurations. A CE amplifier uses $R_L = 200\Omega$. The h-parameters are $h_{ie} = 1100\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 22\ \mu A/V$. Calculate i) Current gain; ii) Input impedance **(06 Marks)**

4 a. What is Miller effect? Draw the high frequency transistor a.c. equivalent circuit (π-Model) and explain the significance of each component in the model. **(08 Marks)**

b. What are the factors that influence the low frequency and high frequency response of a CE – BJT amplifier? **(06 Marks)**

c. Calculate the overall lower 3dB and upper 3dB frequencies for a 3 stage amplifier having an individual lower 3dB frequency of 30 Hz and upper 3dB frequency of 2.5 MHz. **(06 Marks)**

5 a. Why do we cascade amplifiers? State the various methods of cascading transistor amplifiers. A given amplifier arrangement has the following voltage gains. $Av_1 = 10$. $Av_2 = 20$ and $Av_3 = 40$. What is the overall voltage gain? Also express each gain in dB and determine the total voltage gain in dB. **(08 Marks)**

b. Explain the operation and characteristics of cascade and Darlington pair connections. **(04 Marks)**

c. Explain the concept of feedback amplifier. If an amplifier has a bandwidth of 200 kHz and a voltage gain of 80, what will be the new bandwidth and gain if a negative feedback of 5% is introduced? **(08 Marks)**

6 a. How are power amplifier classified? Explain. Show that the transformer coupled class A amplifier has a maximum efficiency of 50%. **(08 Marks)**

b. With circuit diagram, explain the working of class B push pull amplifier. Obtain an expression for the maximum conversion efficiency. **(07 Marks)**

c. What is harmonic distortion? A transistor supplies 0.85 Watts to a 4kΩ load. The zero signal d.c. collector current is 31 mA and the d.c. collector current with signal is 34 mA. Determine the percentage second harmonic distortion. **(05 Marks)**

7 a. State Barkhausen criteria for sustained oscillations and apply this to R.C phase shift oscillator and explain. Write the expression for the frequency of oscillation. Design the R.C. elements of a weinbridge oscillator for operation at $f_o = 10$kHz. **(08 Marks)**

b. With the help of a circuit diagram, explain the working of Hartely oscillator. A colpitt's oscillator is to generate a frequency of 800 kHz. The capacitors to be used to have capacitance $C_1 = 100$ pF and $C_2 = 10$pF. Find the value of inductance. **(06 Marks)**

c. What is frequency stability in oscillators? What factors affect the frequency stability? Explain how crystal oscillator provides good frequency stability. **(06 Marks)**

8 a. What is a JFET and how does it differ from BJT? Explain the different methods of biasing FET. **(07 Marks)**

b. Explain the operation of JFET amplifier. Draw the FET small signal model. Calculate the transconductance g_m of a JFET having values of $I_{DSS} = 12$ mA and $V_p = -4$V at bias points i) $V_{GS} = 0$V; ii) $V_{GS} = -1.5$V. **(06 Marks)**

c. Draw a diagram showing the constructional features of a MOSFET. From the diagram explain in brief how the voltage at the gate controls the flow of carriers. A depletion MOSFET has $I_{DSS} = 12$ mA and $V_P = -4.5$ V. Calculate the drain current at gate source voltages of i) OV; ii) –2V; iii) –3V. **(07 Marks)**